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For Immediate Release

**Cypress Launches IP Oasis™ Support Site to Accelerate Time-to-market
of Communications Applications Using Delta39K CPLDs**

***IP Oasis™ Section on Cypress Web Site Lists
Five New Optimized CPLD Netlists of Mentor Graphics Inventra™ IP Cores***

SAN JOSE, Calif., October 10, 2000 – Cypress Semiconductor (NYSE: CY) today officially launched the IP Oasis™ support site for its Delta39K family of complex programmable logic devices (CPLDs). IP Oasis offers five new Inventra™ Intellectual Property (IP) cores from Mentor Graphics (NASDAQ: MENT), designed to help shorten the time-to-market of communications systems designed using Delta39K CPLDs. The five Inventra cores currently available are the first of a long series of cores specifically designed to take advantage of Cypress's CPLD architectures.

The IP Oasis site was designed to be the primary portal for IP cores targeted at Cypress's Delta39K CPLDs. The cores will be available as optimized netlists. Located at <http://www.cypress.com/pld/ipoasis>, IP Oasis allows users to view and select prequalified intellectual property cores and directs visitors to the Inventra site for license and download. This collaboration results in a complete, e-business-based CPLD solution.

"IP Oasis supports Cypress's strategy to offer a total solution, especially as CPLDs emerge as a viable alternative to FPGAs," said Rich Kapusta, Cypress's programmable logic product marketing manager. "The Delta39K family are the first CPLDs to offer IP cores, enabling our customers to shorten and simplify their overall design cycle and accelerate their time-to-market."

"Inventra's participation in IP Oasis reinforces Mentor's strategy to provide easy, web-based access to optimized CPLD netlists of selected cores," said Sheri Andrew, product marketing manager, Mentor Graphics Inventra IP Division. "Optimized Inventra cores will allow designers to make key system changes late in the development cycle, avoiding costly and time-consuming silicon re-spins. In addition, access to a proven library of IP allows designers to focus on differentiating their end-product solutions, rather than engineering common functions."

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Available IP Cores

The following Inventra CPLD IP cores are available as optimized netlists on IP Oasis:

DMAxN-B1 – This core is a single-channel implementation of the Inventra DMAxN controller soft core, suited to communications processors, microprocessor peripherals and memory management units.

HDLC-CORE-B1 – This IP is an implementation of the Inventra single-channel HDLC-CORE controller soft core, containing a full-duplex transceiver with independent receive and transmit sections for bit-level HDLC protocol operations. It is ideal for networking devices such as hubs, routers and frame relay processors.

M16550A-B1 – Derived from the Inventra M16650A soft core, and targeted at a wide variety of serial communications devices, this core is a high-performance universal asynchronous receiver/transmitter (UART) with two 16-bit FIFOs, one each for transmit and receive.

M16x50-B1 – Highly suited to a range of serial communications devices, this core is an extension of the Inventra M16550A UART with FIFOs and enhancements that emulate features found in various discrete devices.

MI2C-B1 – This IP provides an interface between a microprocessor and an I2C bus, and is often used in consumer appliances such as set-top boxes and audio-video devices. It can be programmed to operate either as a master or slave device; in master mode it performs arbitration to allow its operation in multi-master systems.

Customers who wish to view the data sheets for these netlists can access them through the Cypress Web site at <http://www.cypress.com/pld/ipoasis> or the Mentor Web site at http://www.mentor.com/inventra/netlist_program/cypress_cpld_program.html.

These cores are optimized for use in both Cypress's HDL-based *Warp*™ and Mentor's FPGA Advantage™ design tools, which are tailored to meet the needs of high-end CPLD designers. Both design tools integrate graphical capture, simulation, synthesis, and management, replacing the traditional multi-vendor, multi-tool approach to CPLD or FPGA design.

Cypress Delta39K Family of CPLDs

Cypress Semiconductor's Delta39K CPLD – manufactured using 0.18-micron, 6-layer metal technology – is the world's largest and most feature-rich CPLD. Offering from 15,000 to 350,000 gates, it is the first to offer embedded memory elements, including optimized FIFO and dual-port memory blocks. These memory elements enable fast performance for buffering in data communications applications, as well as fast data storage and retrieval in memory intensive applications.

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Delta39K CPLDs have built-in Spread Aware™ PLL capability, providing board de-skew and clock synchronization. Spread Aware spread-spectrum technology allows the Delta39K IC to interface easily with the other low EMI components on the customer's board. Cypress's innovative Self-Boot™ solution eliminates the need for an external boot PROM, saving valuable board space and making the Delta39K a truly integrated one-chip solution.

Licensing and Availability

These netlists can be licensed for \$5,000 each per use through the Mentor Graphics Web site at (http://www.mentor.com/inventra/netlist_program/cypress_cpld_program.html). Mentor's e-commerce solution is available 24/7 and is being offered to CPLD users for the first time.

About Mentor Graphics Corp.

Mentor Graphics Corporation (Nasdaq: MENT) is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world's largest electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of more than \$500 million and employs approximately 2,600 people worldwide. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777, Silicon Valley headquarters are located at 1001 Ridder Park Drive, San Jose, California 95131-2314. World Wide Web site: www.mentor.com.

About Cypress

Cypress Semiconductor is "Driving the Communications Revolution"™ by providing high-performance integrated circuit solutions to fast-growing markets, including data communications, telecommunications, computation, consumer products, and industrial control. With a focus on emerging communications applications, Cypress's product portfolios include networking-optimized and micropower static RAMs; high-bandwidth multi-port and FIFO memories; high-density programmable logic devices; timing technology for PCs and other digital systems; and controllers for Universal Serial Bus (USB). Cypress is No. 1 in the USB and clock chip markets.

More than two-thirds of Cypress's sales come from fast-growing communications markets and dynamic companies such as Alcatel, Cisco, Ericsson, Lucent, Motorola, Nortel Networks, and 3Com. Cypress's ability to mix and match its broad portfolio of intellectual property enables targeted, integrated solutions for high-speed systems that feed bandwidth-hungry Internet applications. Cypress aims to become the preferred silicon supplier for Internet switching systems and for every Internet data stream to pass through at least one Cypress IC.

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Cypress employs more than 4,100 people worldwide with international headquarters in San Jose, California. Its shares are listed on the New York Stock Exchange under the symbol CY. More information about Cypress is accessible electronically on the company's worldwide web site at <http://www.cypress.com> or by CD-ROM (call 1-800-858-1810). An electronic investor forum, and other investor information, is located at <http://www.cypress.com/investor/index.html>.

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